AN INTERFACE FOR SYNCHRONOUS DATA TRANSFER BETWEEN DOMAINS CLOCKED AT DIFFERENT FREQUENCIES

Field of the Invention

The present invention is related to integrated circuits, and more particularly to an interface for synchronous data transfer between domains, circuits, systems or the like clocked at different frequencies when the clocks are derived from the same high frequency source.

Background Information

What is needed is an interface that will permit the synchronous transfer of data between different domains, circuits, systems or the like that are clocked at different frequencies with minimal latency and error free transfer of the data.

Transfer of data between domains clocked at different frequency ratios is possible with a circular First-In-First-Out (FIFO) buffer. However, this transfer is asynchronous creating latency in the transfer of the data which can adversely affect the speed or efficiency of performance of the domains, circuits or systems operating at different clock frequencies that need to communicate with each other. Input data from the sending domain is strobed or written into the FIFO buffer at the data rate of the sending domain with a "write pointer," and the data is read or transferred to the receiving domain at the data rate of the receiving domain by a "read pointer." The control logic controlling the transfer of data must be programmed to prevent the "write pointer" from overtaking the "read pointer" and vise versa. The size of the buffer and difference between the two frequency domains are important considerations for efficient and error free data transfer.

Summary of the Invention

In accordance with the present invention, an interface for synchronous data transfer between domains clocked at different frequencies includes a first latch for receiving data from a first domain clocked at one frequency when the first latch is

selected and a second latch for receiving data from the first domain when the second latch is selected. A third latch is provided for transferring data from either the first latch or the second latch to the second domain clocked at another frequency. The third latch is toggled to receive data from either the first or second latch in response to a negative edge of a clock pulse of the second domain. Data is also alternately loaded in either the first or second latch from the first domain for transfer to the second domain when the second domain is clocked.

In further accordance with the present invention, a method for synchronous data transfer between clocked domains includes: loading a first master latch with data from the first domain in response to a first domain clock pulse; transferring the data loaded in the first master latch to the second domain through a slave latch in response to a second domain clock pulse; toggling the slave latch to switch to receive data from a second master latch in response to a negative edge of the clock pulse of the second domain clock; loading the second master latch with data from the first domain in response to another first domain clock pulse; transferring the data loaded in the second master latch to the second domain through the slave latch in response to another second domain clock pulse; toggling the slave latch to switch to receive data from the first master latch in response to the negative edge of the clock pulse of the second domain clock; repeating a cycle of alternately loading the first and second master latches and transferring data to the second domain through the slave latch until a master clear (MC) signal is received by the slave and master latches. At least one non-operate or hold state is entered during each repeated cycle for at least one clock pulse of the faster domain clock to prevent the faster clocked domain from overrunning the slower clocked domain.

Brief Description of the Drawings

Figure 1 is block diagram showing a primary source clock and how secondary clocks of different frequencies are derived from the primary clock source.

Figure 2A is a schematic diagram of a sequencer in Figure 1 further illustrating how secondary clocks of different frequencies are derived from a primary clock source.

Figure 2B is a schematic diagram illustrating how a half cycle phase shift is generated in the timing diagrams associated with Figure 2 A.

Figure 3 is a schematic diagram of a secondary sync pulse sequencer for deriving secondary sync clocks for generating clock pulses of different frequencies and pulse widths.

Figure 4 is a schematic diagram of a basic sequencer element.

Figure 5 is a schematic diagram of an interface circuit for transferring data from a first domain clocked at one frequency to a second domain clocked at a different frequency in accordance with the present invention.

Figure 6 is a timing diagram of the operation of the interface circuit of Figure 5 illustrating data transfer from a domain clocked at one frequency to a domain clocked at a slower frequency for different sync clock frequency ratios of the first and second domain clocks.

Figure 7 is a state diagram of the sequence of operation illustrated in Figure 6.

Figure 8 is a timing diagram of the operation of the interface circuit of Figure 5 illustrating the timing for data transfer from a first domain clocked at one frequency to a second domain clocked at a faster frequency for different sync clock frequency ratios of the first and second domain clocks.

Figure 9 is a state diagram of the sequence of operation illustrated in Figure 8.

Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Referring initially to Figure 1, a primary clock source 12 is connected to a group of sequencers 14, 16 and 18 for generating secondary clocks 20, 22 and 24 for driving different elements, circuits or domains (not shown in Figure 1) in a system or device of which the primary clock source 12 and sequencers 14, 16 and 18 and clocks 20, 22 and 24 form a part. The primary clock 12 is a stable, high frequency and symmetrical source. The primary clock 12 is connected to the sequencers 14, 16 and 18 through a

balanced fanout 19 to reduce scaler clock skew between the sequencers. A reset 26 is used to synchronously reset the sequencers 14, 16 and 18 to set all the sequencers in "lock step" during initialization of the circuit to guarantee that the secondary clocks 20, 22 and 24 will be in synchronization. The sequencers 14, 16 and 18 are respectively coupled to "clk A" 20, "Sync Pulse" 22 and "clk B" 24 by a balanced fanout tree with matching delays to insure the synchronization between the clocks 20, 22 and 24 and therefore synchronous low skew data transfer between domains clocked respectively by "clk A" 20 and "clk B" 24. Sync Pulse 22 is a sync message or pulse which will be used by "clk A" 20 and "clk B" 24.

Figure 2A is a detailed schematic diagram of an example of a sequencer 28 that may be used for the sequencers 14, 16 and 18 of Figure 1 to derive the secondary synchronous clocks 20, 22 and 24 operating at different frequencies. The sequencer 28 includes a set master and slave latch, flip flop or the like 30 and series of reset master and slave latches, flip flops or the like 32. The output of each of the master and slave latches 30 and 32 generate a clock pulse waveform that is phase or time shifted as shown in the timing diagram associated with Figure 2A. The clock pulses may be selected by a multiplexer or selector 34 to provide the desired clock pulse width and frequency. Examples of divide by 4 (/4), divide by 5 (/5) and divide by 6 (6/) clock frequency waveforms are shown in Figure 2A.

Figure 2B illustrates how a half cycle shift is generated from the master and slave flip flop 32. A clock distribution that provides a 50% duty cycle is used. The master and slave latches receive inverted clocks that provide for triggering on the pulse edges. The match latch C' output is used to obtain the half cycle phase shift C'.

Figure 3 is a further example of a secondary sync pulse sequencer 28' illustrating how secondary clock pulse waveforms of different frequencies for driving different circuits or domains within a system or device can be derived. Figure 3 further illustrates how the Sync Pulse is generated for different ratios of high to low clock pulse frequencies. For example, the Sync Pulse for a clock pulse ratio of 5:4 (200 Mhz to 166 Mhz) is generated by selecting the S+T+A+B outputs; the clock pulse ratio for 3:2 is generated by selecting K+L+A+B; and the clock pulse ratio for 1:1 is generated by selecting C+D+A+B.

Figure 4 shows an example of a basic sequencer element 30 or 32 for use in the

sequencers 28 and 28' of Figures 2A and 3. The basic sequencer element 30, 32 includes a master/slave flip flop 36. The slave output S is feed back to the input of a multiplexer or selector 38 and multiplexed with an input labeled "D." The output 40 of the multiplexer 38 is feed to the input of a second multiplexer 42 where the output 40 of multiplexer 38 may be multiplexed with a 0 or 1 input. A "HOLD" function is provided with multiplexer 38 and a "SET/RESET (S/R)" function is provided with multiplexer 42. Each flip flop 30, 32 of all sequencers preferably have this functionality to permit synchronous reset and stop clock features.

In accordance with the present invention, shown in Figure 5 is an interface 44 for permitting synchronous data transfer between a first domain 46 clocked at one frequency by a secondary clock 50 and a second domain 48 clocked at another frequency by a secondary clock 52. Each of the domain clocks 50 and 52 are derived from the same high frequency source as previously described with respect to Figures 1-3. The interface 44 includes a first master and slave flip flop or the like 54 and a second master and slave flip flop or the like 56, each connected to the first domain 46. The master latches 54a and 56a of flip flops 54 and 56 are each respectively directly coupled to an input of the associated slave latch 54b and 56b of the flip flops 54 and 56. The Slave latch output for each flip flop 54, 56 is respectively feed back to a multiplexer or selector 58, 60 at the input of each master latch 54a and 56a, respectively. The Slave latch output is then multiplexed with any data from the first domain 38 loaded into either master latch 54a or master latch 56a. The master latch output of master latch 54a labeled "A" and the master latch output of master latch 54b labeled "B" are multiplexed into a slave latch 62 by a multiplexer or selector 64 at the input to the slave latch 62. The multiplexer 64 and slave latch 62 gate or transfer data loaded from the first domain 46 into either the master latch 54a or the master latch 56a into the second domain 48 as will be described in more detail herein.

The operation of the interface 44 for transferring data from the first domain 46 clocked at one frequency to the second domain 48 clocked at a slower frequency or clock speed is described by referring to the three sets of timing diagrams in Figure 6. Each set of waveforms represents a different ratio of clock frequencies between the first initially to the 3:2 ratio waveforms or timing diagrams, the first domain 46 is clocked at 200 Mhz and the second domain 48 is clocked at 133 Mhz. The synch pulse is derived

so that it begins and ends coincident with the negative edges of the faster domain clock in this case the 200 Mhz clock. As shown in Figure 6 the secondary clocks 50 and 52 for the first domain 46 (200 Mhz) and the second domain 48 (133 Mhz) are repeated in a systematic pattern with each cycle being framed by the sync pulse (vertical broken lines 66 and 6A8). An ABsel signal is generated to alternately select either the master latch 54a of flip flop 54 or the master latch 56a of flip flop 56 for loading data from the first domain 46. For simplicity of explanation in reference to Figures 5 and 6, the output "A" of the master latch 54a corresponds to clock pulses also labeled "A" in Figure 6. When an "A" clock pulse occurs in the 200 Mhz waveform clocking the first domain 46, data will be loaded into the master latch 54a and when an "A" clock pulse occurs in the slower frequency waveform (160 Mhz, 133 Mhz or 100 Mhz) the data loaded in the master latch 54a will be transferred or gated to the second domain 48 through the slave latch 62. Similarly, the output "B" of the master latch 56a for flip flop 56 corresponds to clock pulses also labeled "B" in Figure 6. When a "B" pulse occurs in the 200 Mhz waveform clocking the first domain 46, data will be loaded into the master latch 56a and when a "B" pulse occurs in the slower frequency waveform clocking the second domain, the data loaded in the master latch 56a will be transferred or gated to the second domain 48 from slave latch 62. . The ABsel select signal is generated to select the other of master latches 54a or 56a in response to or by a positive edge of an "A" or "B" pulse for loading data into one of the master latches 54a or 56a. For example, when a "B" pulse occurs clocking the first domain 46, data is loaded into the master latch 56a and the interface 44 is switched to the master latch 54a for receiving data when the next "A" pulse occurs. Similarly, the interface 44 will switch to the master latch 56a after an "A" pulse so that data can be loaded into the master latch 56a when the next "B" clock pulse occurs.

In the repeating pattern of Figure 6, the master latch 56a is initially selected or enabled by ABsel to receive data from the first domain 46. Data is then received or loaded into into the master latch 56a from the first domain 46 when the first domain is clocked by the 200 Mhz clock 50 as shown by the first "B" pulse 70 of the 200 Mhz clock waveform in Figure 6. After loading data into the master latch 56a the signal ABsel is generated to switch from master latch 56a to master latch 54a when the first domain 46 is next clocked for transferring data.

Slave latch 62 alternately looks at the outputs A and B of latches 54a and 56a, respectively. Because of the sync pulse 72, the second domain 48 will be synchronously clocked by a first "B" pulse 74 of the 133 Mhz clock 52 and the slave latch 62 will immediately transfer the data to the second domain 48. The negative edge 76 of the 133 Mhz "B" pulse will cause a signal ABtransfer (Figure 5) to be generated to toggle the slave latch 62 to look or switch to the "A" output of the master latch 54a.

The next clock pulse 78 of the 200 Mhz clock 50, designated "A" in Figure 6, will cause data from the first domain 46 to be loaded into the master latch 54a. The data in master latch 54a will then be transferred to the second domain 48 when the second domain 48 is clocked by the next clock pulse 80 of the 133 Mhz clock 52, correspondingly designated as "A" on the 133 Mhz waveform in Figure 6 to indicate correspondence with the "A" output of the master latch 54a. The negative edge 82 of the 133 Mhz "A" pulse will cause the signal ABtransfer to be generated to toggle the slave latch 62 to look or switch to the "B" output of the master latch 56a.

To prevent a race condition or the faster domain overrunning the slower domain and to force average data transfer rates and minimal latency, the next clock pulse of the 200 Mhz clock is designated as a "non-operate" (NOP) pulse 84 during which no data is loaded or transferred.

The waveforms labeled "A" and "B" in Figure 6 illustrate the time frames when data is valid for master latch 54a (A output) and master latch 56a (B output) and when the data is unreliable or uncertain as indicated by the "XXX" or cross-hatching. These periods occur after a toggle between master latches 54a and 56a when data is to be loaded into the other master latch.

As evident from Figure 6, the cyclical pattern will continue with data being loaded alternately into master latch 54a or master latch 56a from the first domain 46 and transferred to the second domain 48 when the second domain 48 is clocked by a next or subsequent clock pulse. By examination, it can be seen that the 5:4 and 2:1 ratio frequency differences between the second and first domains 46 and 48 operate in the same manner. By comparing the 3:2 waveforms to the 5:4 and 2:1 waveforms, it is apparent that the present invention works for various ratios of clock frequency differences for transferring data between domains clocked at different frequencies.

Figure 7 is a state sequence diagram illustrating the different operational states

for transferring data between the first and second domains 46 and 48 and further illustrates the repeating pattern for loading data into master latches 54a and 56a and transferring the data to the second domain 48. The sequence can be initialized or restarted by a master clear, mc=1, to reset the latches 54, 56 and 62. The sequence will then begin again when mc=0 and a sync pulse is received.

Referring now to Figure 8, a timing diagram for Figure 5 is shown illustrating the transfer of data from the domain 46 to the second domain 48 in which the first domain is clocked by a slower clock (160 Mhz, 133 Mhz or 100 Mhz) compared to the second domain which is clocked by a faster clock, in this case 200 Mhz. The interface 44 will operate analogously to the previously described examples were data is being transferred from a faster clocked domain to a slower clocked domain (Figure 6). Referring to the 3:2 set of waveforms, the first "A" pulse 86 of the 133 Mhz waveform will permit data to be loaded into the master latch 54a from the first domain 46 in Figure 5. Because of the sync pulse 88, the second domain 48 is synchronously clocked by the "A" pulse 90 of the second domain clock 52, operating at 200 Mhz in this example and the data is immediately transferred into the second domain 48 via slave latch 62. As before, the negative edge of the second domain clock pulse will cause the slave latch 62 to toggle to look at the other of the "A" or "B" output of the master latches 54a and 56a. Accordingly, the negative edge 92 of the "A" clock pulse 90 of the 200 Mhz clock will cause the slave latch 62 to switch to the "B" output of master latch 56a. To coordinate data transfer from the first and second domains 46 and 48 in this example of going from a slower clocked domain to a faster clocked domain, the next clock pulse 94 of the faster second domain clock 52 will be designated as a "HOLD" or non-operate (NOP) pulse to permit the slower clocked domain to catch up or keep up. The next "B" pulse 96 of the 133 Mhz first domain clock 50 will permit data from the first domain 46 to be loaded into the master latch 56a. The ABsel signal will be generated to toggle to master latch 54a to receive data when the first domain 46 is clocked by the next "A" pulse 98. When the second domain 48 is clocked by the next "B" pulse 100 of the second domain 200 Mhz clock 52, the data loaded into master latch 56a will be transferred via slave latch 62 to the second domain 48. As before, the negative edge 102 of the second domain "B" clock pulse 100 will generate the signal ABtransfer to cause the slave latch 62 to switch to the "A" output of master latch 54a to

receive data when the next "A" pulse 104 of the second domain clock 52 occurs.

Those of skilled in the art will recognize that the 5:4 and 2:1 ratio frequencies will operate analogously to that just described with respect to the 3:2 frequency ratio.

Figure 9 is a state diagram illustrating the different states of operation for transferring data from a first domain 46 clocked at one frequency to a second domain 48 clocked at as faster frequency as illustrated by the timing diagrams in Figure 8.

One example of an application of the present invention is were the first domain 46 may be a memory controller IC clocked at one rate or frequency that synchronously communicates with a memory, the second domain 48, that may be clocked at several possible rates. The present invention thus provides synchronous data transfer for several frequency ratios with a single design. This means that a migratory memory upgrade path is achieved without the need for costly IC redesigns and with the benefits of synchronous performance.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.